(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 431 180 A1**

(12) **EUROPEAN PATENT APPLICATION published in accordance with Art. 158(3) EPC**

(21) Application number: **90908659.7**

(51) Int. Cl.[5]: **G05B 19/415**

(22) Date of filing: **30.05.90**

(86) International application number:
PCT/JP90/00711

(87) International publication number:
WO 90/16022 (27.12.90 90/29)

(30) Priority: **20.06.89 JP 157281/89**

(43) Date of publication of application:
12.06.91 Bulletin 91/24

(84) Designated Contracting States:
DE FR GB

(71) Applicant: **FANUC LTD.**
3580, Shibokusa Aza-Komanba, Oshino-mura
Minamitsuru-gun, Yamanashi 401-05(JP)

(72) Inventor: **KOKURA, Masuo**
1-18-16, Asahigaoka Hino-shi
Tokyo 191(JP)
Inventor: **ITO, K Fanuc Dai-3 Vira-karamatsu**
3527-1, Shibokusa, Oshinomura
Minamitsuru-gun
Yamanashi 401-05(JP)

(74) Representative: **Brunner, Michael John et al**
GILL JENNINGS & EVERY 53-64 Chancery Lane
London WC2A 1HN(GB)

(54) **AXIS CONTROL SYSTEM OF NUMERICAL CONTROL APPARATUS.**

(57) An axis control system of a numerical control apparatus comprising first and second microprocessors (11,21) for interpolating the axes of dissimilar constitutions, and first and second interpolation signal generating circuits (17, 27) provided for the respective microprocessors to generate interpolation period signals. An output signal (D_o) of the first microprocessor and an interpolation period signal (ITP1) of the first interpolation signal generating circuit are input to the second interpolation signal generating circuit (27). An interpolation period signal in synchronism with the first interpolation signal generating circuit (17) is generated based on the logic of these signals. When the interpolation period signals are brought into synchronism, the first and second microprocessors (11,21) execute the interpolation of axes of respective axis constitutions.

EP 0 431 180 A1

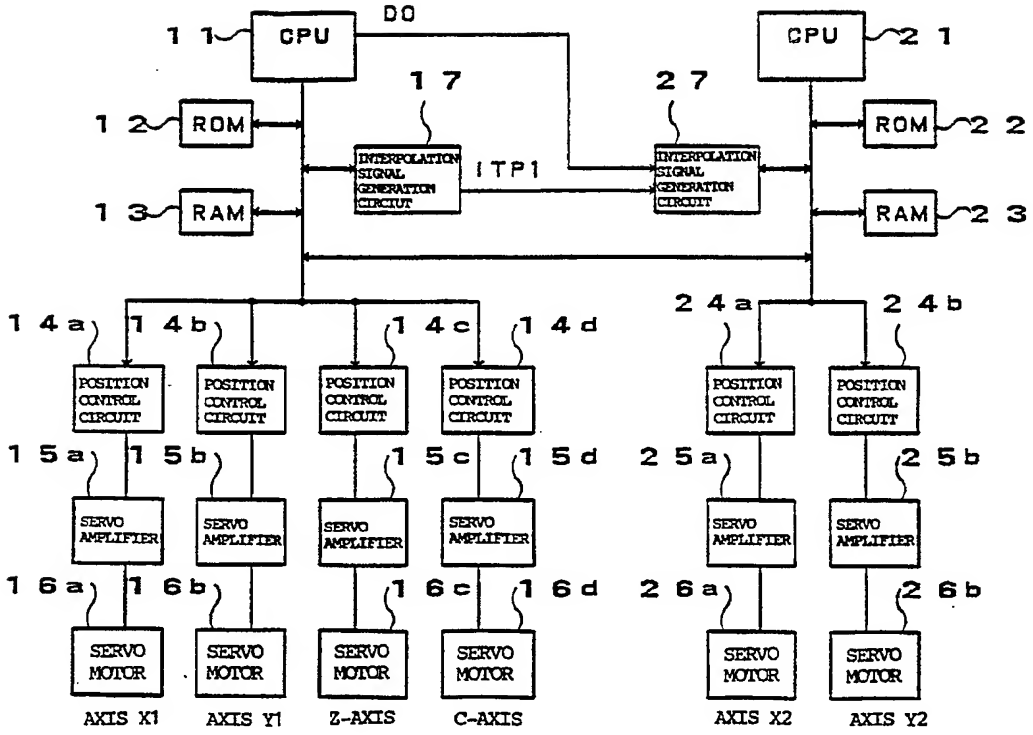
CPU
DO
11
17
27
CPU
21
12
ROM
INTERPOLATION SIGNAL GENERATION CIRCUIT
ITP1
INTERPOLATION SIGNAL GENERATION CIRCUIT
ROM
22
13
RAM
RAM
23
14a
14b
14c
14d
24a
24b
POSITION CONTROL CIRCUIT
15a
15b
15c
15d
25a
25b
SERVO AMPLIFIER
16a
16b
16c
16d
26a
26b
SERVO MOTOR
AXIS X1
AXIS Y1
Z-AXIS
C-AXIS
AXIS X2
AXIS Y2

Fig. 1

AXIS CONTROL SYSTEM FOR NUMERICAL CONTROL APPARATUS

TECHNICAL FIELD

The present invention relates to an axis control system for a numerical control apparatus, and more specifically, to an axis control system for a numerical control apparatus by which a plurality of microprocessors (CPUs) interpolate axes that each have a different axis arrangement.

BACKGROUND ART

Numerical control apparatuses which control a multiplicity of axes or spindles are widely used to effect machining at a high speed. This type of the numerical control apparatus contains a plurality of microprocessors (CPUs), and the axes to be controlled are assigned to each CPU, respectively. More specifically, each CPU has an independent axis arrangement, and therefore, the axes to be controlled by each CPU are prefixed, and the axes which can be interpolated by each CPU are fixed by the axis arrangement thereof.

The prior art will be described below with reference to the drawings, wherein Figure 4 shows a prior art axis control system for a numerical control apparatus.

A CPU 11 controls an axis arrangement composed of an axis X1 an axis Y1, a Z-axis, and a C-axis; a CPU 21 controls an axis arrangement composed of an axis X2 and an axis Y2; ROMs 12 and 22 are composed of an EPROM or an EEPROM and store the system program of the CPUs 11 and 21; and RAMs 13 and 23 are composed of a SRAM or the like and store various data or input/output signals. Although not shown, a non-volatile memory supplied with power from a battery, a graphic control circuit, a display, an operator's panel and the like are connected to the CPUs 11 and 21, through a bus, in addition to the above-described units.

Each axis is composed of a position control circuit, a servo amplifier, and a servo motor, and since the respective axes have the same arrangement, only the axis X1 will be described here.

A position control circuit 14a receives a position command from the CPU 11 and outputs a speed command signal to a servo amplifier 15a for controlling a servo motor 16a. The servo amplifier 15a amplifies the speed command signal and drives the servo motor 16a.

Although not shown, a position sensor for outputting a position feedback signal and a tachometer generator for outputting a speed feedback signal are connected to the servo motor 16a, respectively. A pulse coder or the like is used as the position sensor to feed back a position feedback pulse to the position control circuit 14a. The tachometer generator feeds back a voltage signal in accordance with a rotational speed of the servo motor 16a to the servo amplifier 15a.

Interpolation signal generation circuits 17 and 27 count a system clock supplied thereto and output an ITP (interpolation) cycle signal at a predetermined timing. The ITP (interpolation) signal output is usually made at intervals of 8 milliseconds. The CPUs 11 and 21 manage an interpolation processing time in response to the interpolation cycle signal.

The CPU 11 is connected to the CPU 21 through a bus, and data is exchanged therebetween through the bus.

In the prior art axis control system, since the ITP (interpolation) cycle signal serving as an interpolation criterion is created by the respective different interpolation signal generation circuits 17 and 27, the CPUs 11 and 21 generate the interpolation cycle signal at a different timing. As a result, a problem arises in that the CPU 11 can control the axis x1, the axis Y1, the Z-axis, and the C-axis, but cannot control the axis x2 and the axis Y2, whereas the CPU 21 can control the axis X2 and the axis Y2, but cannot control the axis x1, the axis Y1, the Z-axis, and the C-axis.

DISCLOSURE OF THE INVENTION

Taking the above into consideration, an object of the present invention is to provide an axis control system for a numerical control apparatus, by which a plurality of microprocessors for interpolating axes that each have a different axis arrangement can arbitrarily select axes to be interpolated, respectively.

To solve the above problem, according to the present invention, there is provided an axis control system for a numerical control apparatus having first and second microprocessors for interpolating axes that each have a different axis arrangement and first and second interpolation signal generation circuits provided with each of the microprocessors for generating an interpolation cycle signal, which comprises the second interpolation signal generation circuit receiving an output signal from the first microprocessor and the interpolation cycle signal from the first interpolation signal generation circuit and generating an interpolation cycle signal synchronized with the first interpolation signal generation circuit based on a logic of the received signals.

The second interpolation signal generation circuit receives the output signal from the first microprocessor and the interpolation cycle signal from

the first interpolation signal generation circuit. The second interpolation signal generation circuit does not generate an interpolation cycle signal until receiving the interpolation cycle signal from the first interpolation signal generation circuit after it has received the output signal from the first microprocessor. Then, upon reception of the interpolation cycle signal from the first interpolation signal generation circuit, the second interpolation signal generation circuit generates the interpolation cycle signal. With this arrangement, the first and second interpolation signal generation circuits generate a synchronized interpolation cycle signal, and when the interpolation cycle signal is synchronized, the first and second microprocessors can interpolate the axes that each have a different axis arrangement.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a diagram showing a schematic arrangement of an embodiment of an axis control system for a numerical control apparatus according to the present invention;

Figure 2 is a diagram showing the detailed arrangement of an interpolation signal generation circuit;

Figures 3(a) and 3(b) are diagrams showing a timing of the operation of the interpolation signal generation circuit; and

Figure 4 is a diagram showing a prior art axis control system for a numerical control apparatus.

BEST MODE OF CARRYING OUT THE INVENTION

An embodiment of the present invention will be described below with reference to the drawings.

Figure 1 is a diagram showing a schematic arrangement of an embodiment of an axis control system for a numerical control apparatus according to the present invention. Since the same numerals as used in Figure 4 are used to designate the same elements, a description thereof is omitted.

In the present embodiment, an output signal DO from a CPU 11 and an interpolation cycle signal ITP1 from an interpolation signal generation circuit 17 are output to an interpolation signal generation circuit 27. The interpolation signal generation circuit 27 receives these signals DO and ITP1 and creates an ITP (interpolation) cycle signal ITP2 synchronized with the interpolation signal generation circuit 17.

Figure 2 is a detailed diagram of arrangement of the interpolation signal generation circuit 27.

An interval timer counter 28 receives a system clock of 1 microsecond and outputs an interpolation cycle signal to an AND circuit 29 at every 8000 counts. When an output from a logic circuit 30 is at a high level "1", the AND circuit 29 outputs the interpolation cycle signal ITP2 from the interval timer counter 28. The interval timer counter 28 is reset in response to the interpolation cycle signal ITP2 from the AND circuit 29.

The logic circuit 30 receives an ITP continuation signal from a CPU 21, the output signal DO from the CPU 11, and the interpolation cycle signal ITP1 from the interpolation signal generation circuit 17, and outputs the logical result thereof to the AND circuit 29.

The ITP continuation signal is defined as a signal to be output when the interpolation cycle signal ITP2 received by the CPU2 has been interpolated. Therefore, if the ITP continuation signal is not at a high level "1", the high level "1" cannot be output to the AND circuit 29.

Further, the logic circuit 30 sets the output therefrom to a low level "0" by receiving the output signal DO from the CPU1, and the logic circuit 30 set to the low level "0" in response to the output signal DO from the CPU1 is reset by receiving the interpolation cycle signal ITP1 from the CPU1 and outputs a high level "1" to the AND circuit 29. Therefore, when the output signal DO from the CPU1 is input to the logic circuit 30, the AND circuit 29 cannot output the interpolation cycle signal ITP2 even if the interval timer counter 28 outputs a high level "1". The AND circuit 29 outputs the interpolation cycle signal ITP2 as soon as the interpolation cycle signal ITP1 is input to the logic circuit 30.

The operation of the interpolation signal generation circuit 27 will be described below with reference to the drawings. Figures 3(a) and 3(b) show a timing of the operation of the interpolation signal generation circuit 27.

In Figure 3(a), although the interpolation cycle signal ITP1 from the interpolation signal generation circuit 17 and the interpolation cycle signal ITP2 from the interpolation signal generation circuit 27 are output at a cycle of 8 milliseconds, but these signals are generated at a different timing. When the output signal DO from the CPU1 is input to the logic circuit 30, the logic circuit 30 outputs a low level "0", regardless of the ITP continuation signal from the CPU2, until the interpolation cycle signal ITP1 is input, and as soon as the interpolation cycle signal ITP1 is output, the interpolation cycle signal ITP2 synchronized with the interpolation cycle signal ITP1 is output.

In Figure 3(b), the interpolation cycle signals ITP1 and ITP2 are synchronized with each other and output at the same timing. At this time, even if the same time is needed for the CPU 2 to effect the interpolation, accordingly and an output of the ITP continuation signal from the CPU1 is delayed,

the interpolation signal generation circuit 27 outputs an interpolation cycle signal ITP2 which is a shifted synchronization with the interpolation cycle signal ITP1. More specifically, the synchronization of the interpolation signals can be shifted to match a shift in the synchronization caused by the interpolation processing time. Note, even if the synchronization is shifted as described above, the interpolation cycle signals ITP1 and ITP2 can be resynchronized by an operation similar to that of Figure 3(a).

As described above, according to the present invention, even if the interpolation signal generation circuits generate signals at a different timing, the signals can be easily synchronized, and even if the timing of the signals is shifted by the state of an interpolation processing after the synchronization has been achieved, the interpolation processing can be carried out in the state where the synchronization of the signals has been shifted.

In the above embodiment, the case in which the interpolation signal generation circuit 27 is synchronized is described, but the interpolation signal generation circuit 17 may be synchronized or both interpolation signal generation circuits may have the same arrangement and any one of the interpolation signal generation circuits may be synchronized.

As described above, according to the present invention, interpolations signals from interpolation signal generation circuits provided with each microprocessors can be synchronized, and thus a plurality of the microprocessors for interpolating axes that each have a different axis arrangement can arbitrarily select the axes to be interpolated, respectively.

Claims

1. An axis control system for a numerical control apparatus having first and second microprocessors for interpolating axes having a different axis arrangement each other and first and second interpolation signal generation circuits provided with each of said microprocessors for generating an interpolation cycle signal, characterized wherein:
said second interpolation signal generation circuit receiving an output signal from said first microprocessor and said interpolation cycle signal from said first interpolation signal generation circuit and generating an interpolation cycle signal synchronized with said first interpolation signal generation circuit based on a logic of said received signals.

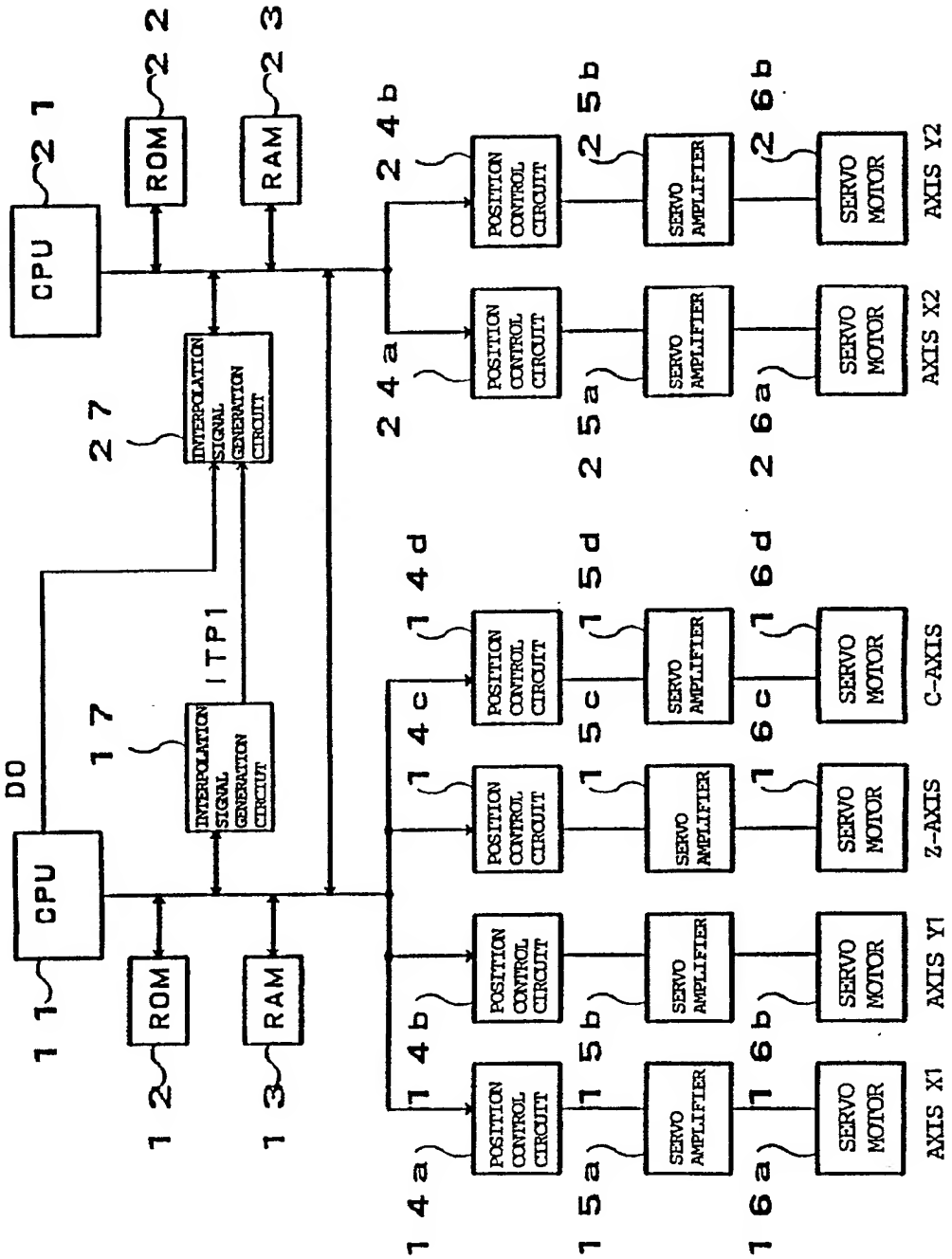
CPU
ROM
RAM
INTERPOLATION SIGNAL GENERATION CIRCUIT
POSITION CONTROL CIRCUIT
SERVO AMPLIFIER
SERVO MOTOR
AXIS X1
AXIS Y1
Z-AXIS
C-AXIS
AXIS X2
AXIS Y2
ITP1
D0

Fig. 1

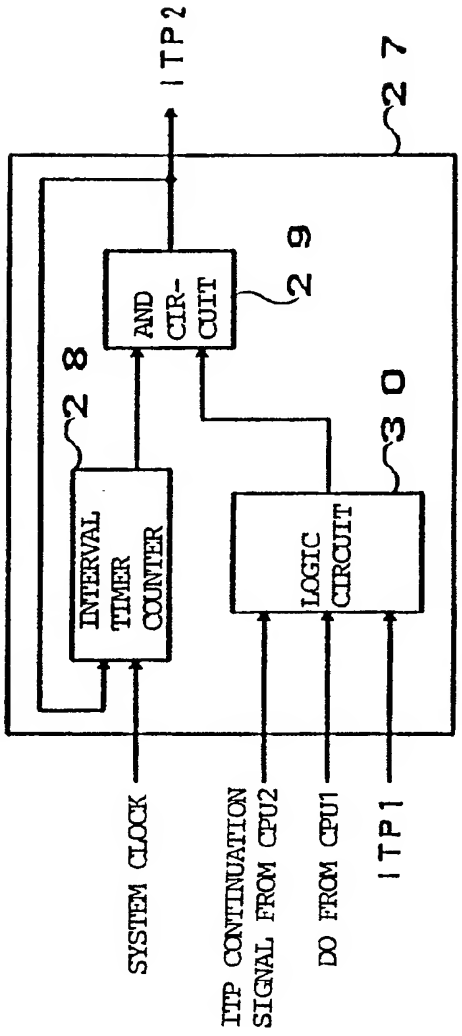
ITP2
27
29
AND CIR-CUIT
28
30
INTERVAL TIMER COUNTER
LOGIC CIRCUIT
SYSTEM CLOCK
ITP CONTINUATION SIGNAL FROM CPU2
DO FROM CPU1
ITP1

Fig. 2

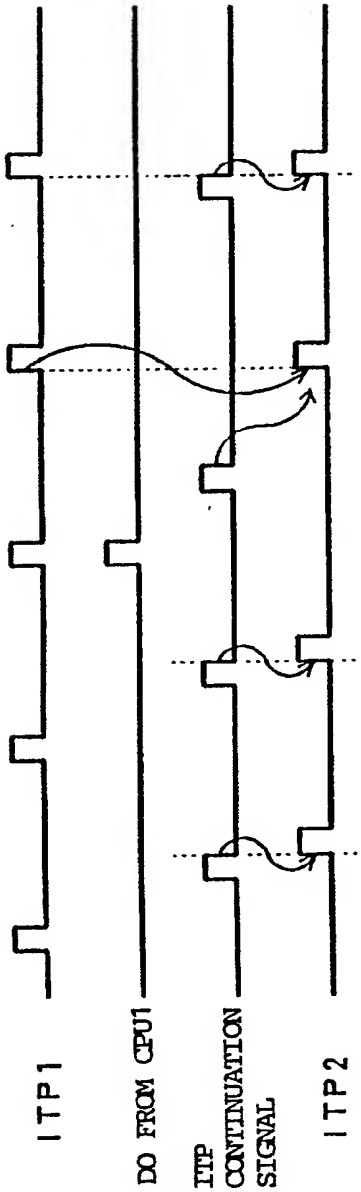
ITP1
DO FROM CPU1
ITP
CONTINUATION
SIGNAL
ITP2

Fig. 3 (a)

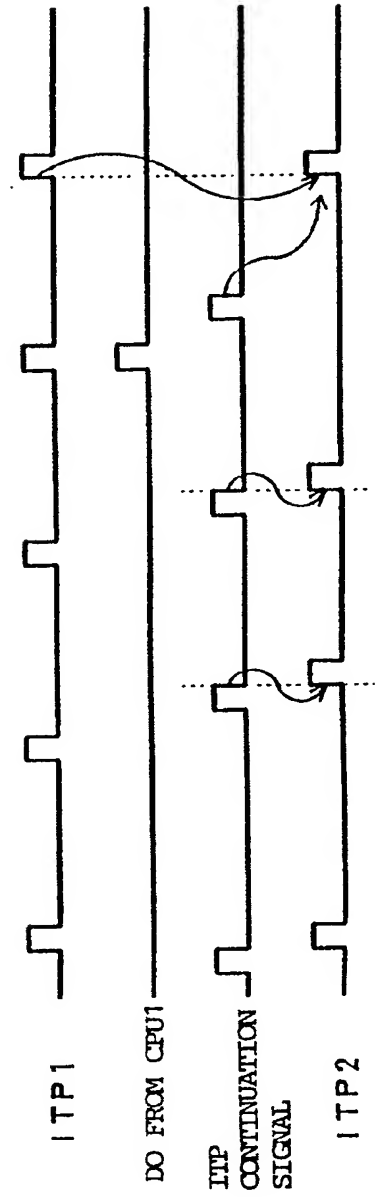
ITP1
DO FROM CPU1
ITP
CONTINUATION
SIGNAL
ITP2

Fig. 3 (b)

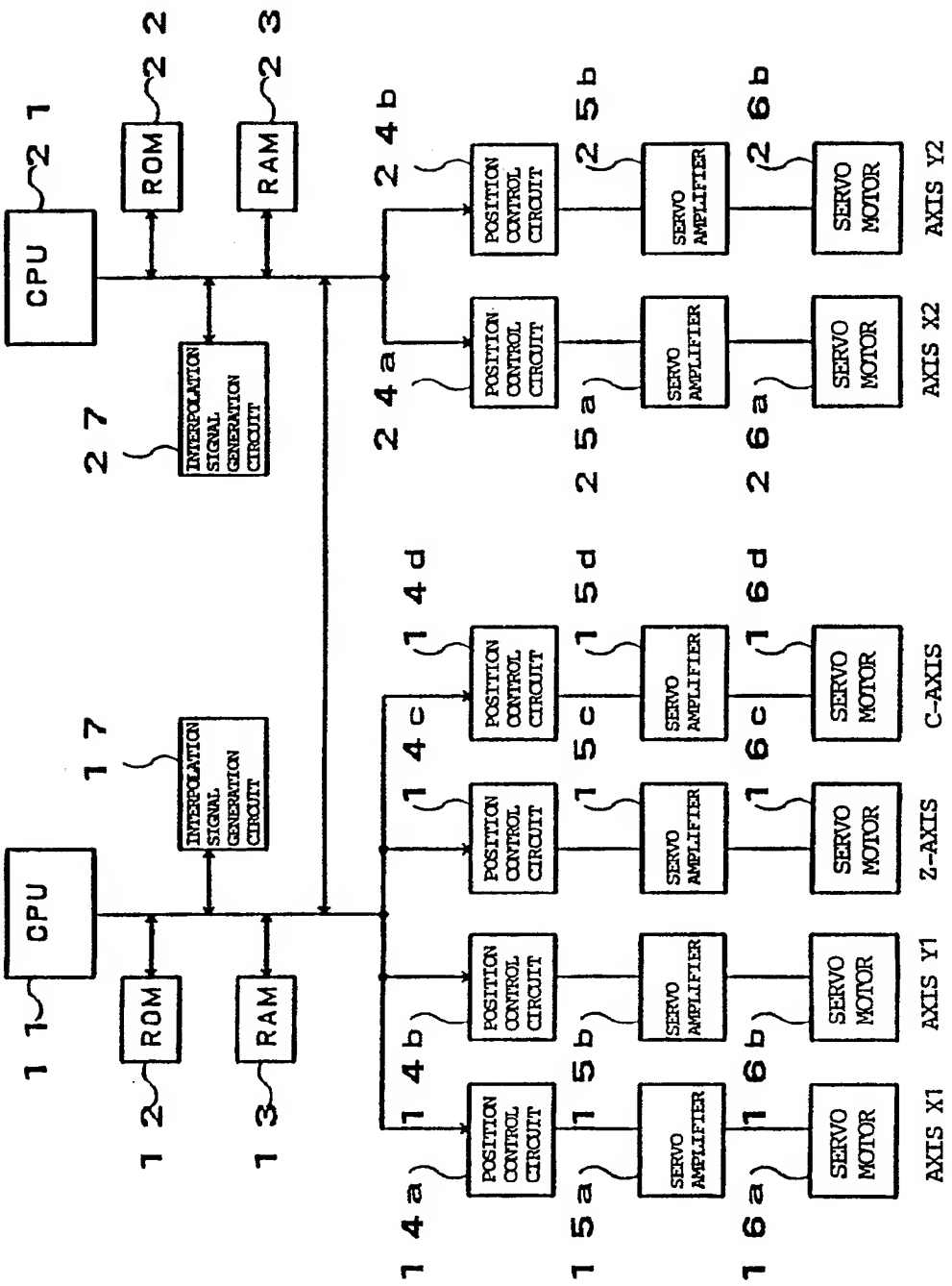
CPU
ROM
RAM
INTERPOLATION SIGNAL GENERATION CIRCUIT
POSITION CONTROL CIRCUIT
SERVO AMPLIFIER
SERVO MOTOR
AXIS X1
AXIS Y1
Z-AXIS
C-AXIS
AXIS X2
AXIS Y2

Fig. 4

INTERNATIONAL SEARCH REPORT

International Application No PCT/JP90/00711

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int. Cl[5] G05B19/415

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC	G05B19/415, G05B19/19

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

Jitsuyo Shinan Koho 1932 - 1990
Kokai Jitsuyo Shinan Koho 1971 - 1990

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
Y	JP, A, 60-45808 (Nippon Sheet Glass Co., Ltd., DIGI-Tech Laboratory, K.K.), 12 March 1985 (12. 03. 85), (Family: none)	1
Y	JP, A, 63-237106 (Mikuni Kogyo K.K.), 3 October 1988 (03. 10. 88), (Family: none)	1
A	JP, A, 60-200311 (Yasukawa Electric Mfg. Co., Ltd.), 9 October 1985 (09. 10. 85), (Family: none)	1

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
August 29, 1990 (29. 08. 90)	September 10, 1990 (10. 09. 90)

International Searching Authority	Signature of Authorized Officer
Japanese Patent Office	